REMARKS

Applicant respectfully requests reconsideration of the above identified application. Claims 1-30 are pending. Claims 1-30 are rejected.

Applicant respectfully notes that in the Office Action mailed on December 19, 2003, interpretations or characterizations by the Examiner include inferences and/or potential limitations, to which Applicant does not agree.

35 U.S.C. § 102 REJECTIONS

The Office Action mailed on December 19, 2003 rejects Claims 1-30 under 35 U.S.C. 102(e) as allegedly being anticipated by US Pat. No. 6,192,467 (Abdallah).

The Examiner states with regard to Claims 1-30 and especially with regard to 28-30 that Abdallah teaches, "(b) an execution unit responsive to the first instruction (col. 6, line 59) to shuffle 16-bit data elements from the source operand to the destination operand," then stating that, "the shuffle operation was well known; see Sidwell." The Examiner further states that, "(c) wherein the source and destination operand are the same operand or the processor is comprised of hardware and software components," were well known. Applicant respectfully disagrees with the Examiners assertions.

Further, to anticipate a claim, a prior art reference must disclose every limitation of the claimed invention, either explicitly or inherently. In re Schreiber, 128 F.3d 1473, 1477, 44 USPQ2d 1429, 1431 (Fed. Cir. 1997). If the

Examiner intends to combine references, for example Abdallah and Sidwell, then Applicant respectfully submits that an anticipation rejection under 35 U.S.C. 102 is not proper. Accordingly in light of the argument presented above, Applicant respectfully requests the Examiner withdraw the rejection of Claims 1-30 for allegedly being anticipated by Abdallah.

It is respectfully noted that Claim 22 was not rejected on the basis of any reference other than Abdallah. Therefore, Applicant believes the subject matter of Claim 22 is allowable.

The Office Action rejects Claims 1-21 and 23-25 under 35 U.S.C. 102(b) as allegedly being anticipated by US Pat. No. 5,819,117 (Hansen).

The Examiner states with regard to Claims 17-21 that Hansen teaches, "(b) generating a first portion of the destination operand comprised of the data elements from the same portion of the source operand (fig. 3B)," and that, "(c) wherein the portion is either the upper half or lower half (bytes zero to three) of the source and destination operands, which can be the same operand." Applicant respectfully disagrees.

Hansen admits that Figures 3A and 3B show 4-byte L. E. (Little Endian) and B. E. (Big Endian) load operations, respectively, from memory to processor register 12 (col. 6, lines 31-44). Applicant respectfully submits that in a 32-bit load from a 32-bit source memory operand into a 64-bit destination register operand, the portion of the register operand (half) is not the same as the portion of the memory operand (all). Further the portion is neither the upper nor the lower half of the memory operand. Finally, Hansen does not explicitly disclose or suggest that in his load or store operations, the source and destination operands can be the same. In fact, Hansen admits that his load and store operations are between the processor's registers and its memory system (col. 3,

lines 21-24) and that in the case in which the processor and memory system have different byte ordering schemes, a byte permutation unit rearranges the bytes of the transferred data (col. 3, lines 54-58).

Accordingly in light of the argument presented above, Applicant respectfully requests the Examiner withdraw the rejection of Claims 17-21 for allegedly being anticipated by Hansen.

The Examiner states with regard to Claims 1-16 and 23-25 that Hansen (figs. 3B and 10C) teaches, "(c) access a packed data operand (71) having at least two portions... (d) select a set of data elements from a portion of the packed data operand... (e) copy each data element of the selected set of data elements to specified data fields located in the corresponding portion of the destination operand (74), (f) wherein the packed data operand includes eight data elements... (g) wherein... the data elements of 16-bits to 128 bit operands and the same destination operand," the latter of which the Examiner states are, "all well known."

Applicant respectfully submits that Figures 3B and 10C show 4-byte B. E. (Big Endian) load operations from memory to a processor register (col. 6, lines 31-44 and col. 14, lines 56-58). Applicant respectfully submits that data elements of the 32-bit source memory operand are not copied into a corresponding portion of the 64-bit destination register, for example, all of the memory operand is copied into the lower half of the destination register. Further, Hansen does not disclose or suggest that in his L. E. (Little Endian) and B. E. (Big Endian) load or store operations the data elements are 16-bits. Finally, Hansen does not disclose or suggest that in his load or store operations, the source and destination operands can be the same. Accordingly in light of the argument presented

above, Applicant respectfully requests the Examiner withdraw the rejection of Claims 1-16 and 23-25 for allegedly being anticipated by Hansen.

The Office Action rejects Claims 26 and 27 under 35 U.S.C. 102(b) as allegedly being anticipated by US Pat. No. 5,822,619 (Sidwell).

The Examiner states with regard to Claims 26 and 27 that Sidwell teaches, "(a) decoding a single instruction (col. 9, line 51) specifying a source operand of 128 bits," and that, "(b) responsive to the single instruction and the control word, shuffling 16-bit data element[s] from the source operand... (fig. 9; col. 8, line 1)." Applicant respectfully disagrees.

Sidwell, at col. 9, line 51, admits that zip4n2v1p interleaves objects from a 64-bit source operand. Figure 9 also clearly shows 64-bit zips and unzips from a 64-bit source operand rather than a 128-bit source operand as claimed by Claims 26 and 27 (Fig. 9; col. 8, lines 59-64). Sidwell further admits that his computer has several important qualities, one being that source operands are always the natural word length of 64 bits (col. 4, lines 56-65).

Therefore, at least in light of the above arguments, Applicant respectfully requests the Examiner withdraw the rejection of Claims 26 and 27 for allegedly being anticipated by Sidwell.

The Office Action also rejects Claims 26 and 27 under 35 U.S.C. 102(e) as allegedly being anticipated by US Pat. No. 6,288,723 (Huff) and US Pat. No. 6,115,812 (Abdallah).

With regard to Huff (and Abdallah), which has a common assignee and inventor with the present application, Applicant reserves the right to submit a showing under 37 CFR 1.131 and/or 37 CFR 1.132 to overcome the rejection. Alternatively though, Applicant respectfully wishes to point out that Figs. 3D and 3E illustrate the operations of shuffle packed single instructions (SHUFPS),

which belong to FP Instruction Set 118 of Fig. 1 (col. 6, lines 25-26 and 43-44). Applicant believes that Huff (and Abdallah) discloses explicitly, at least, operations of shuffle packed single instructions (SHUFPS) to operate on single precision 32-bit floating point data elements (col. 5, lines 32-36) rather than on 16-bit data elements as claimed by Claims 26 and 27.

Accordingly, Applicant respectfully requests the Examiner withdraw the rejection of Claims 26 and 27 for allegedly being anticipated by Huff.

Therefore, Applicant respectfully submits that Claims 1, 6, 11, 17, 20, 23, 26 and 28 are patently distinguished over the art cited by the Examiner. Applicants further believe that Claims 2-5, 7-10, 12-16, 21-22, 24-25, 27 and 29-30 being dependent therefrom are also patentable. Applicants respectfully request the Examiner withdraw his rejections under 35 U.S.C. 102.

Applicants, therefore, believe that Claims 1-30 are presently in condition for allowance and such action is earnestly solicited.

CONCLUSION

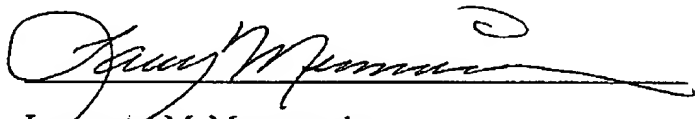
Applicants respectfully submit the present claims for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call Lawrence M. Mennemeier at (408) 765-2194.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Date: 4-13-04



Lawrence M. Mennemeier

Reg. No. 51,003

12400 Wilshire Boulevard

Seventh Floor

Los Angeles, CA 90025-1026

(408) 720-8300